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Abstract: Optoelectronic imaging of integrated-circuits has revolutionized device design debug, failure analysis and electrical fault isolation; however modern probing techniques like laser-assisted device alteration (LADA) have failed to keep pace with the semiconductor industry's aggressive device scaling, meaning that previously satisfactory techniques no longer exhibit a sufficient ability to localize electrical faults, instead casting suspicion upon dozens of potential root-cause transistors. Here, we introduce a new high-resolution probing technique, two-photon laser-assisted device alteration (2pLADA), which exploits two-photon absorption (TPA) to provide precise three-dimensional localization of the photo-carriers injected by the TPA process, enabling us to implicate individual transistors separated by 100 nm. Furthermore, we illustrate the technique's capability to reveal speed-limiting transistor switching evolution with an unprecedented timing resolution approaching <10 ps. Together, the exceptional spatial and temporal resolutions demonstrated here now make it possible to extend optical fault localization to sub-14 nm technology nodes.

OCIS codes: (180.4315) Nonlinear microscopy; (320.7090) Ultrafast lasers; (130.5990) Semiconductors.

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1. Introduction

Dynamic laser stimulation (DLS) [1] enables a variety of state-of-the-art integrated-circuit (IC) diagnostic solutions, which address the challenges of spatially localizing performance-limiting circuit failures within CMOS nanoelectronic circuits. Based on the acquisition of either laser-induced photo-electric or photo-thermal functional test mapping, these precision through-substrate technologies traditionally utilize a continuous-wave (CW) 1064 nm or 1340 nm laser source, respectively, in order to abate experimental complexity and cost. Specifically, continuous laser interrogation guarantees temporal overlap between the incident optical radiation and a preconditioned electrical tester stimulus configured to exercise the device. Examples of such analytical optoelectronic probing platforms include soft defect localization (SDL) [2] and laser-assisted device alteration (LADA) [3]. These advanced modalities function by coaxing operationally sensitive transistors to advance or delay their switching characteristics in order to alter the pass / fail outcome of a pre-determined marginal test stimulus. This outcome provides vital information for globally localizing, with diffraction-limited precision, areas of the chip whose designs limit its overall speed. However, the absence of temporal information overlooks an important dimension associated with speed-limiting performance, and consequently the semiconductor failure-analysis community is beginning to develop novel time-resolved, applications-driven laser probing methodologies for interrogating nanoscale flip-chip architectures in order to refine the silicon validation cycle.

Recently, Erington *et al* addressed this challenge by using a software-enhanced CW laser scanning microscope (LSM) to extract timing information from pixel-shifted data originating from LADA images captured at different scan rates with a temporal resolution on the order of μs [4]. In addition, Perdu *et al* described a modulated CW laser-assisted fault localization approach which could glean a few nanoseconds of functional timing information from a device under test (DUT) [5]. Although impressively innovative, these extended CW techniques are ultimately limited by their reliance on conventional optical sources. Therefore, the adoption of advanced mode-locked laser systems is required to extend these technologies into the ultrafast temporal domain. Douin *et al* may have recognized this by utilizing a picosecond laser system to demonstrate time-resolved DLS imaging whilst observing signal propagation along an 860 MHz ring oscillator structure [6]. This was implemented by employing the mode-locked laser repetition rate as the timing reference for the DUT clock stimulus.

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In this article, we describe how two-photon carrier injection at photon energies just below the bandgap can be used to configure a novel time-resolved ultrafast optical probing tool for the qualitative and quantitative characterization of critical timing path analysis in a silicon IC. This was facilitated by combining TPA within the active layer of the DUT with a pulse-to-DUT synchronization scheme whereby the arrival of femtosecond laser pulses could be locked and temporally shifted with respect to the internal clock frequency of a DUT with picosecond precision. We show how this technique delivers a significant advance in the spatio-temporally resolved probing of silicon ICs, and furthermore how undesirable effects associated with traditional LADA are eliminated, such as scattered photons from surrounding metal layers and structures, and thermal interactions due to CW 1064 nm interrogation.

2. Failure localization to individual transistors using 2pLADA

The test vehicle adopted was a proprietary 28 nm bulk-silicon test device (V_{dd} = 0.8 V, clock frequency = 50 MHz) containing production logic blocks. To exercise the device, a production scan test, lasting 21 μs, was modified to engineer a race condition – as illustrated in Fig. 1. Data were launched through a data-path circuit at time t_1 and captured at t_2. The data-path propagation delay, t_p, depends on the power supply voltage, V, and the test is passed if $(t_2-t_1) > t_p(V)$. For LADA, both V and (t_2-t_1), are chosen to make $(t_2-t_1) \approx t_p(V)$, so that the probability of passing the test is naturally 50%. Laser irradiation of any of the circuits affects either the effective clock period or the propagation delay, highlighting sensitive locations by modulating the probability of failure, so providing the ideal conditions for performing LADA.

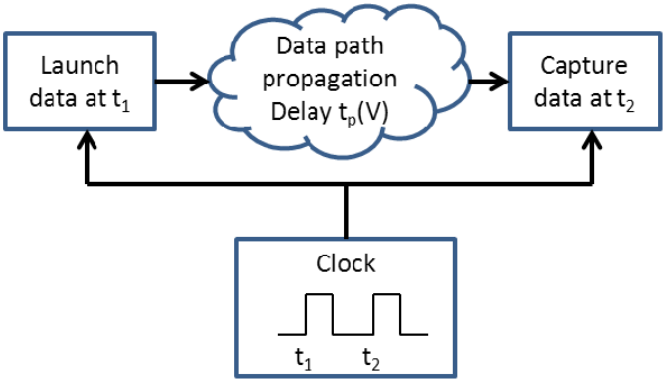

Fig. 1. For LADA, the power supply voltage, V, and the clock period, (t_2-t_1), are chosen to make $(t_2-t_1) \approx t_p(V)$, so that the probability of failing the test is naturally 50%. Laser irradiation of any of the circuits affects either the effective clock period or the propagation delay, highlighting sensitive locations by modulating the probability of failure.

For the 2pLADA work, we employed an ultrafast 1280 nm laser source. This was based on Raman self-frequency shifted soliton generation in a highly nonlinear photonic crystal fiber (PCF) pumped by an efficient mode-locked ytterbium-doped fiber laser (YDFL) [7]. The 1280 nm Raman-soliton pulses were fiber delivered to the LSM with pulse durations of 200 fs and an average power of 20 mW. The repetition frequency was 100 MHz and could be locked to an external 100 MHz clock supplied by the tester. Figures 2(a) and 2(b) illustrate, respectively, the imaging capabilities of a conventional CW 1064 nm LADA system and a 2pLADA system using the 1280 nm ultrafast laser source. The optical power incident on the 2.45 NA GaAs SIL was 0.35 mW for both techniques, and corresponded to a peak power of 17.5 W for the mode-locked laser. Two hundred LADA images of a region containing a simple inverter structure were acquired with a pixel dwell time of 32 μs and an image size of 512 × 512. The fail rate was set to 50%, and the laser pulses (separated by 10 ns) were synchronized to start arriving 3.06 ns after the test loop trigger. It is immediately clear from Fig. 2(a) that the traditional CW 1064 nm LADA methodology is unable to localize its weak

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signal to individual transistor sites, offering instead a global single polarity (i.e. predominantly passing) signal distribution which cannot be overlaid with the accompanying computer-aided design (CAD) details defining the layout of the device's active layers (orange blocks) and poly-silicon gates (green lines).

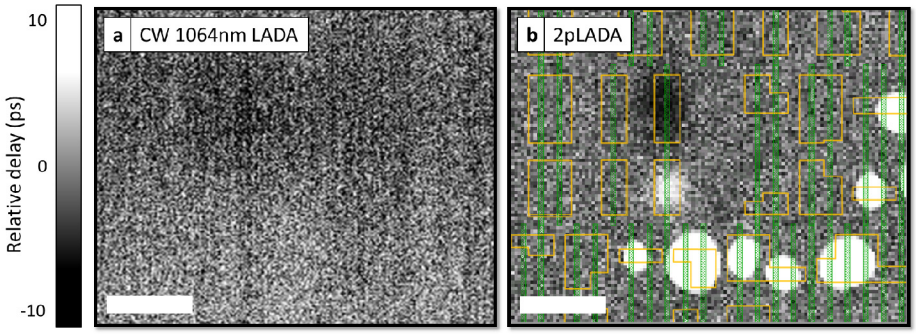

Fig. 2. (a) A CW 1064 nm LADA image and (b), a 2pLADA image. The LADA images were averaged 200 times before visualization. The CAD overlay in (b) highlights the active transistor-area silicon (orange) and poly-silicon gates (green). Horizontal scale bars in (a) and (b), 500 nm.

Under conventional LADA stimulation, such a single polarity signature normally dominates, and its characteristics are typically biased towards the PMOS transistor due to its favorable light-matter interaction sensitivity [3]. By contrast, our results indicate that 2pLADA produces highly localized LADA signatures which, when the incident laser pulse is accurately synchronized in time with the inverter's switching event, emanate from the inverter's individual PMOS and NMOS transistors and do not exhibit strong PMOS dominance – as illustrated in Fig. 2(b). Moreover, with only 0.35 mW incident at the device and averaging of 200 images, it is clear that 2pLADA outperforms its CW 1064 nm LADA counterpart in terms of signal acquisition rate, since the higher peak power of the mode-locked laser pulses makes it possible to perturb and visualize weaker LADA sites without damaging the device. Significantly, these results represent the first LADA embodiment capable of simultaneously generating a complementary time-resolved LADA signal pair, of opposing polarities and of approximately equal signal strengths, at an acquisition rate superior to conventional CW 1064 nm LADA.

3. Two-photon absorption induced single-event upsets

The 2pLADA data in Fig. 2(b) also reveal additional information in the form of a cluster of intense failing sites, which are highly localized to individual transistors within a series of flip-flops and are optically activated as a direct consequence of the high peak power and localized nonlinearity delivered to the device. These unique signatures display incredibly sharp signal transitions which clearly outperform the centrally located 2pLADA sites' when examined under the same conditions. Although captured in a LADA image, these strong electrical signatures do not correspond to the customary pass / fail signals produced by LADA stimulation. Instead, they represent a collection of two-photon absorption induced single-event upset sites (2pSEU). A single-event upset (SEU), which belongs to a wider group of radiation-induced anomalies known as single-event effects (SEE) [8–12], is characterized by the non-permanent perturbation (or, more specifically, change of state) in a microprocessor's functionality caused by an individual node's sensitivity to incident high-energy particles or electromagnetic radiation. These soft errors have been widely studied in many programmable logic devices [13, 14] and have even, as is demonstrated here, been generated through the use of two-photon absorption [15, 16]. However, although linear and nonlinear SEU implementation and characterization are commonplace in the aerospace and defense research communities, the novelty of this particular result originates in the enhanced 2pLADA signal

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extraction methodology, which offers a unique and alternative solution to traditional SEU investigations. Further research is needed before a comprehensive explanation of the underlying mechanism for 2pSEU can be offered.

4. Lateral fault localization performance using 2pLADA

For the purposes of evaluating the 2pLADA lateral spatial resolution performance, we performed a line-cut profile plot, originating at the peak / trough of the LADA fail / pass activation sites, and traversing the edge of each feature until the 2pLADA signal reached the nominal 50% pass / fail background. Using these plots it was possible to fit the integral of a Gaussian point-spread function, whose full-width at half-maximum (FWHM) provided the effective 2pLADA probing resolution [17–19]. From these individual passing and failing 2pLADA sites, FWHM probing diameters of 380 nm (X) and 215 nm (Y) were calculated, respectively. For the incident wavelength of 1.28 μm and an NA = 2.45, the Rayleigh criterion $\Delta x = 0.61\lambda/NA\sqrt{2}$ (modified for two-photon excitation) predicts a lateral resolution of 222 nm, therefore the observed probing resolutions correspond to 1.73 × and 0.98 × the scalar diffraction limit.

The ultimate purpose of LADA and similar techniques is to identify the location of sensitive transistors, so a meaningful distinction can be drawn between the conventional imaging resolution (as discussed above) and the isolation resolution, which quantifies the ability to localize, as opposed to resolve, a signal within a specific area. For this reason, the evaluation of the isolation resolution proceeded by using a separate figure of merit. Figure 3(a) illustrates the same collection of 2pLADA sites in Fig. 3(b); however, instead of accumulating only 200 averages, Fig. 3(a) was constructed from approximately 650 averages in order to suppress the background noise in the data set. A vertical line-cut was performed on this image and the absolute delay profiles of the PMOS and NMOS LADA signals which it provided are presented in Fig. 3(b). The isolation resolution performance can be defined as the physical separation between independently addressable LADA sites. The PMOS and NMOS sites in Fig. 3(a) qualify as independent sites because they exhibit opposite 2pLADA polarities. Measured from the point where the 2pLADA delay reaches the background level, the isolation resolution can be estimated to be 98 ± 5 nm. These sites were known from CAD data to have an actual separation of 117 nm, which is consistent with our experimental value (although slightly outside our uncertainty estimate), and implies that 2pLADA is capable of localizing to an accuracy of approximately half of the diffraction-limited optical resolution.

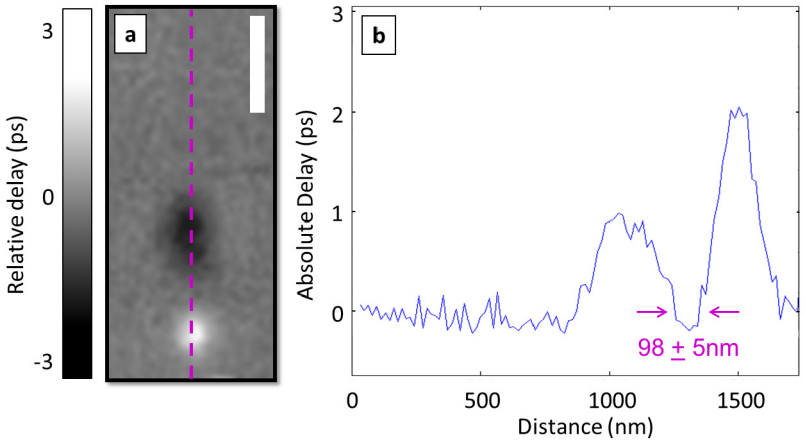

Fig. 3. (a) A 2pLADA image of LADA activation sites using 650 averages and (b), a localized, cumulative, line-cut profile, whose direction is represented by the dashed purple line in (a), representing the absolute delay of the 2pLADA sites. The resulting lateral isolation resolution was measured to be 98 ± 5 nm. Vertical scale bar in (a), 500 nm.

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5. Time-resolved performance in 2pLADA

In addition to the enhanced optoelectronic imaging and fault localization capabilities offered by 2pLADA, the use of synchronized femtosecond laser pulses makes it possible to temporally resolve the switching evolution of individual transistors associated with the electrical test. To demonstrate this we concentrated on two separate circuit features, a NOR gate (Site A) and an inverter (Site B), which were neighboring logical elements in terms of electrical signal propagation. Figure 4(a) illustrates their physical locations in a confocal laser scanning microscope (LSM) image acquired using a 100X objective lens. The strongest 2pLADA images associated with the NOR gate and the inverter are shown in Fig. 4(b) and Fig. 4(c), and were acquired when the incident femtosecond laser pulses were synchronized to arrive at Site A (B) 2.92 ns (3.06 ns) after the test loop trigger, with a timing accuracy approaching <10 ps. These experimental data implied that the electrical LADA stimulus required 140 ps to travel the 97.46 μm interconnect path length linking the two structures – represented by the purple line in Fig. 4(a). This result can be compared against the propagation delay calculated by using a numerical simulation of the circuit's electrical performance based on an assumption of the charge injected into each of the circuit nodes by the femtosecond laser. We found a precise agreement between the experiment and the simulation for an injected charge of 1.2 fC, which can be used to infer an overall two-photon stimulation efficiency of 0.07%, on the basis that two incident photons yield (at most) one photoelectron.

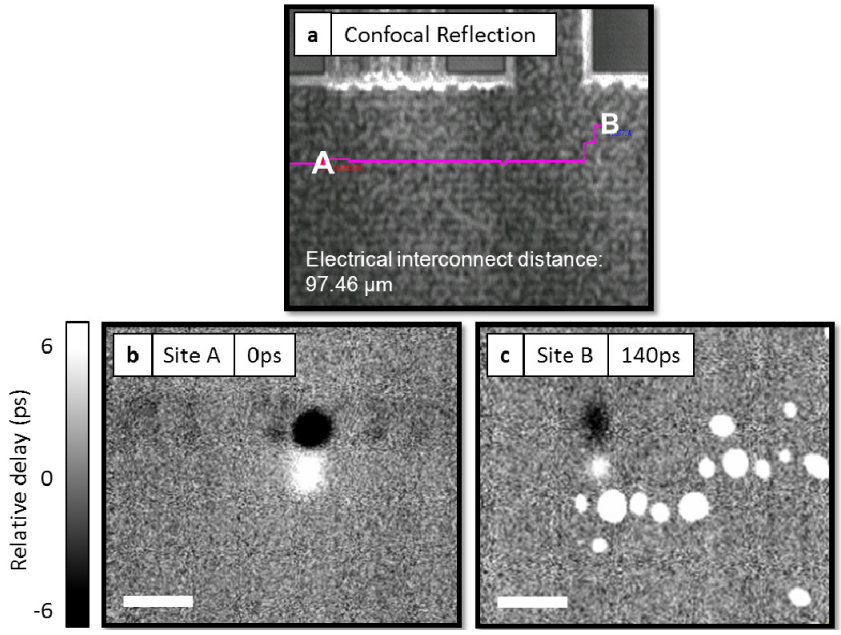

Fig. 4. (a), A confocal reflection image taken using a 1.28 μm confocal LSM and a 100X objective lens to capture the electrical interconnect path, or signal path (represented by the purple line), between Site A (NOR gate) and Site B (inverter). (b), A 2pLADA image of Site A captured at a laser phase interval that represented 0 ps in time and (c), another 2pLADA image of Site B captured approximately 140 ps later, with a timing accuracy in both cases approaching <10 ps. The scale bar indicates the magnitude of laser-induced relative electrical delay generated at each circuit location through 2pLADA. Horizontal scale bars in (b) and (c), 500 nm.

6. Discussion

Several factors contribute to the enhanced performance observed using 2pLADA, the unique benefits of which arise as a natural consequence of the high peak power of the incident

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femtosecond laser pulses, the axial localization of the technique (at an excitation wavelength of 1280 nm, the longitudinal optical FWHM, calculated using $\Delta z = 0.88\lambda/n\sqrt{2}$ [20] - which has been modified for two-photon excitation, where n represents the refractive index of silicon – is approximately 230 nm; however, the axial optoelectronic interaction will be further reduced by LADA's threshold laser power sensitivity to more accurately overlap with the physical longitudinal extent of the transistor's active layer), and the time-resolved capabilities offered by the synchronization scheme. Since the LADA race condition is interrogated for only the duration of the incident optical pulse, photo-generated carriers that are not injected directly into depletion regions have insufficient time to diffuse into the junction and influence the measurement. In addition, the LADA race condition is subject to a threshold interaction level which is sensitive to the energy-density of the injected photo-carriers and the incident laser power, not simply the spatio-temporal laser power profile of the optical pulse. Below a given value of carrier density injection, there will be little or no measured effect on the resulting fail rate. This effect introduces an added complexity into the quantitative analysis of determining LADA resolution performance. There are undoubtedly many additional light-matter and physical semiconductor-device effects influencing the results presented here which require further study. These include the influence on 2pLADA of the polarization dependence of the optical intensity distribution in the focal plane of the high-NA system, and how a non-uniform focal-plane energy-density distribution can manipulate the observed LADA fail rate [17].

7. Conclusion

The results presented here show that 2pLADA has the potential to localize failure sites to a precision of around 100 nm, a performance that significantly exceeds the capabilities of established CW 1064 nm methodologies and is, for the first time, now sufficient to extend optical fault localization to sub-14 nm technology nodes. Improvements in signal generation and collection-rate efficiency have been confirmed, along with the creation of new device evaluation opportunities such as the acquisition of time-lapsed device functionality data, two-dimensional propagation delay mapping, the exclusive separation of optoelectronic activity emanating from confined PMOS and NMOS structures, and the future investigation of 2pSEUs. Not only does 2pLADA establish the state-of-the-art in dynamic nanophotonic silicon device analysis, but it also directly addresses the growing industrial demand for ultrafast time-gated performance.

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